N21
Hardware User Guide

Issue 1.1

Date 2018-09-17

Neoway Product Documentation

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Notice

This document is applicable to N21.

This document is intended for system engineers (SEs), development engineers, and test engineers.

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About This Document

Scope

This document is applicable to N21 series.

It defines the features, indicators, reference designs, and test standards of the N21 module.

Reference designs in this document are only for reference. Customers should design applications based on the actual scenarios and conditions.Please contact Neoway FAE if you have any question or doubt.

Audience

This document is intended for system engineers (SEs), development engineers, and test engineers.

Revision History

Issue	Date	Changes	Revised By
1.0	2018-06	Initial draft	Huang Jianlong
1.1	2018-08	• Updated operating voltage range • Updated temperature ranges • Updated bands supported • Updated pin description	Huang Jianlong

Symbols and Conventions

Symbol	Indication
 Warning	This warning symbol means danger. You are in a situation that could cause fatal device damage or even bodily damage.
 Caution	Means reader be careful. In this situation, you might perform an action that could result in module or product damages.
 Note	Means note or tips for readers to use the module

Related Documents

Neoway_N21_Datasheet

Neoway_N21_Product_Specifications

Neoway_N21_AT_Command_Mannual

Neoway_N21_EVK_User_Guide

1 About N21

1.1 Product Overview

N21 is an compact industrial-grade NB-IoT module that supports Cat NB1.

N21 series include multiple variants. 错误!未找到引用源。 Lists the variants and bands supported.

Table 1-1 Variants and bands

Function	Variant	Network Type	Band
N21	N21-CN-011AS1	Cat NB1	HD-FDD: B3,B5,B8
	N21-EU-011AS1	Cat NB1	HD-FDD: B3,B8,B20
	N21-AP-011AS1	Cat NB1	HD-FDD: B3,B5,B8,B28

Featured with ultra-low power consumption, extensive coverage and simple peripheral circuits, N21 facilitates development and is well applicable to IoT applications that requires low rate and low power consumption.It adopts 22-pin LGA package and its dimensions are 18 mm x 13.8 mm x 2.5 mm, which can meet the size requirement of most customers.

It provides customers the following hardware resources:

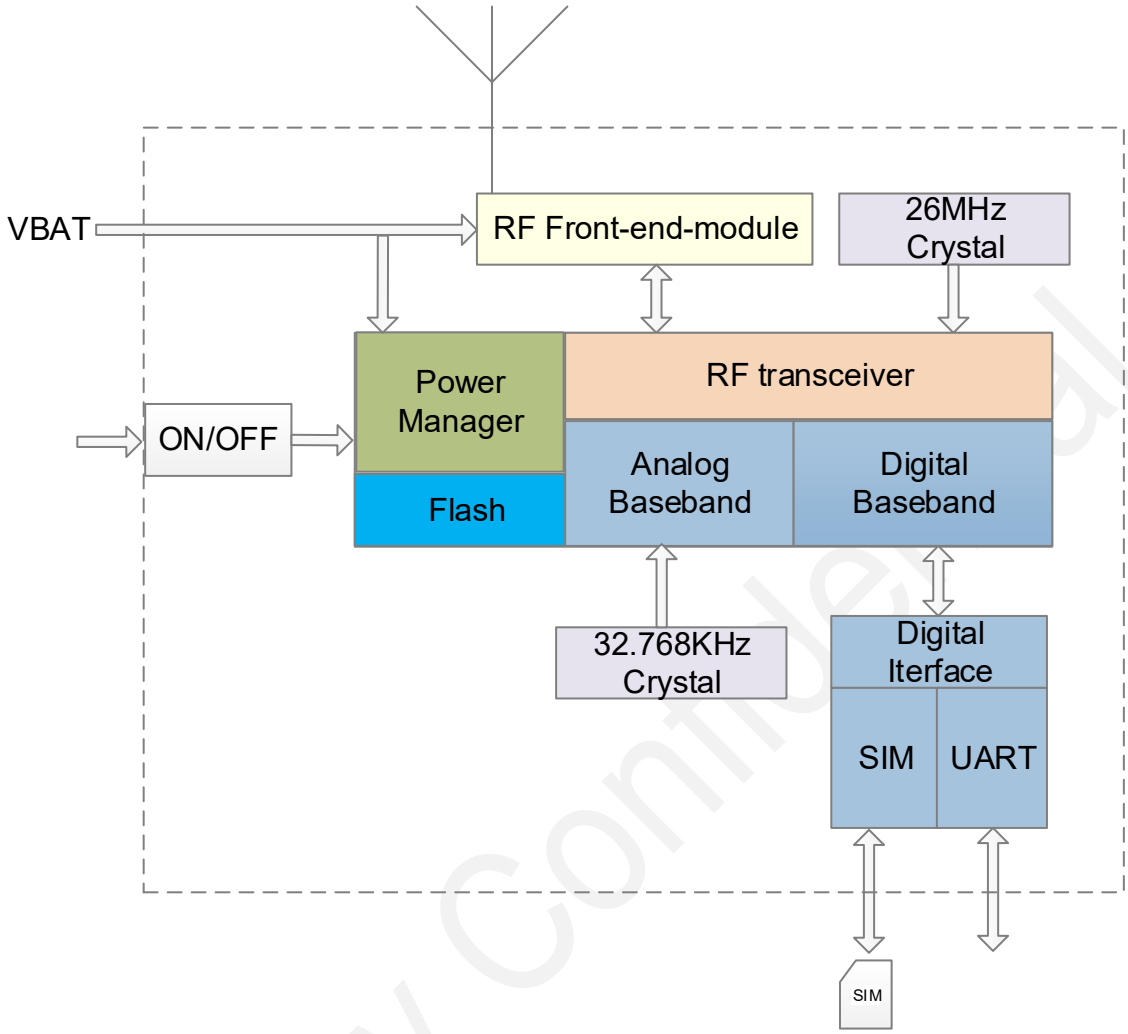
- UART interfaces, used for data communication, firmware update, and commissioning
- Compatible with 1.8 V/3.0V USIM card
- STATUS (working status) /NET_LIGHT (network status indicator)/WAKEUP (PSM wakeup) /RESET

1.2 Block Diagram

N21 consists of the following functionality modules:

- Power management unit
- Clock unit
- Digital interfaces (UIM, UART)
- RF section

Figure 1-1 Block Diagram



1.3 Basic Features

Parameter	Description
Physical features	• Dimensions: (18.0±0.15) mm × (13.8±0.15) mm × (2.5±0.15) mm • Package: LGA • Weight: around 1.3g
Temperature ranges	Operating: -30°C to +75°C Extended: -40°C to +85°C Storage: -45°C to +90°C
Operating voltage	VBAT: 3.1V to 4.3V, TYP: 3.6V
MIPS processor	Main frequency: 192MHz, 16KB L2 cache

Memory	RAM: 32 Mb ROM: 32 Mb
Band	B3, B5, B8, B20, B28
Wireless rate	LTE Cat NB1: 32Kbps (DL) /72Kbps (UL)
Transmit power	LTE: +23dBm+/-2dB(Power Class 3)
Application Interfaces	4G antenna, 50Ω characteristic impedance
	1 UART interface, used to send AT commands
	1 USIM interface, compatible with 1.8V/3V USIM card
	2*2mm embedded eSIM (Optional)
AT commands	3GPP Rel-13 Neoway extended commands
Protocol	TCP/UDP/HTTP/HTTPS/FTP/LWM2M/MQTT/COAP
Certificates and Approvals	CCC, SRRC, CTA, RoHS, CE*, GCF*, Vodafone*, FCC* China Mobile/China Unicom/China Telecom Ali cloud*

* indicates in development

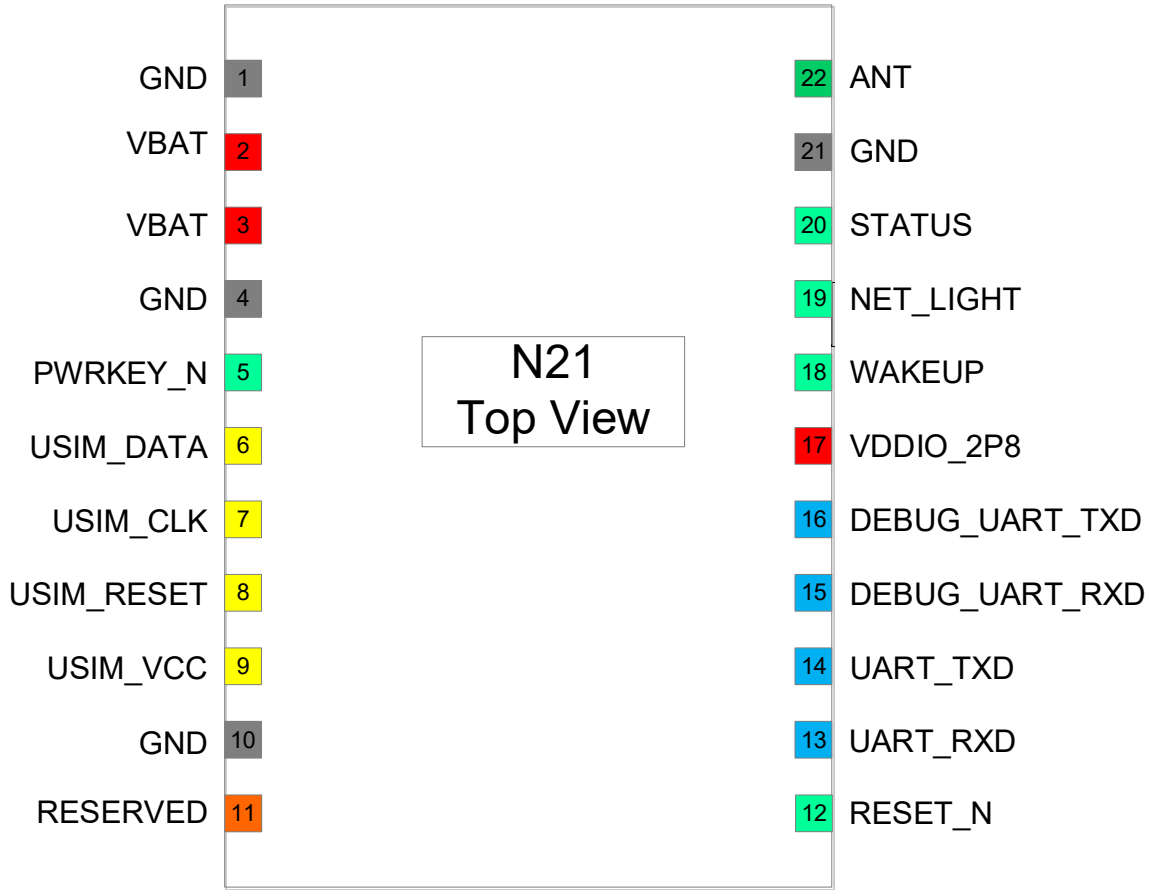
2 Module Pins

There are 22 pins on N21 and their pads are introduced in LGA package.

2.1 Pad Layout

Figure 2-1 shows the pad layout of N21.

Figure 2-1 Pin definition of N21



2.2 Pin Description

Table 2-1 lists the definition of IO types.

Table 2-1 IO definition

IO Type			
DO	Digital output, COMS logic level		
DI	Digital input, COMS logic level		
PO	Power output		
PI	Power supply input		
AO	Analog output		
AI	Analog input		
Level Feature			
P1	1.8V/3.0V	1.8V level feature: V_{IH}=1.26V~1.8V, V_{IL}=-0.3V~0.36V V_{OH}=1.44V~1.8V, V_{OL}=0V~0.4V	3.0V level feature: V_{IH}=2V~3V, V_{IL}=-0.3V~0.57V V_{OH}=2.28V~3V, V_{OL}=0V~0.4V
P2	2.8V digital IO	$V_{IH\ min}$=1.96V, $V_{IL\ max}$= 0.84V $V_{OH\ min}$=2.38V, V_{OLmax}=0.42V	

Table 2-2 Pin Description

Signal	**Pin**	**I/O**	**Function**	**Level Feature**	**Remarks**
Power Supply Pins					
VBAT	2, 3	PI	Main power supply input	V_{max}=4.3V	
VDDIO_2P8	17	PO	2.8V power supply output	V_{norm}=2.8V I_{max}=50mA	Used only for level shifting and IO power supply. Leave this pin unconnected if it is not used.
GND	1, 4, 10, 21				Ensure that all GND pins are connected to the ground.
Control Interfaces					
RESET_N	12	DI	Module reset input	P2	Triggered by low level to

					reset the module.
PWRKEY_N	5	DI	ON/OFF button	P2	Triggered by low level to start or shut down the module.
WAKEUP	18	DI	PSM wakeup input	P2	Input high level for 1 second at this pin and the module will wake up.
STATUS	20	DO	Working status indicator	P2	Leave this pin unconnected if it is not used.
NET_LIGHT	19	DO	Network status indicator	P2	Used together with AT commands
UART Interface					
UART_TXD	14	DO	Data transmitting	P2	Used for data transmission. Leave this pin unconnected if it is not used.
UART_RXD	13	DI	Data receiving	P2	
DEBUG_UART Interface					
DEBUG_UART_RXD	15	DI	Data receiving	P2	Used for commissioning. Leave this pin unconnected if it is not used.
DEBUG_UART_TXD	16	DO	Data transmitting	P2	
USIM interface					
USIM_VCC	9	PO	Power supply output of USIM card	IO_{max} =50mA	USIM_VCC
USIM_DATA	6	DIO	USIM card data IO	P1	
USIM_CLK	7	DO	USIM clock	P1	
USIM_RESET	8	DO	USIM reset	P1	
Antenna Interface					
ANT	22	AI/O	Antenna		50 Ω impedance for traces
Reserved Pins					
RESERVED	11				Leave these pins unconnected. Do not connect them to ground or power supply through a pull-up resistor.

3 Application Interfaces

N21 provides power supply, control, communications, RF, and other interfaces to meet customers requirements in different application scenarios.

This chapter describes how to design each interface and what to note of and provides reference designs.

3.1 Power Supply Pins

The design and PCB layout of the power supply part is the most critical process in application design and they will determine the performance of customers application.Please read the design precaution of power supply and comply with the correct design principles to obtain the optimal circuit performance.

Signal	Pin	I/O	Function	Remarks
VBAT	2, 3	PI	Main power supply input	3.1V~4.3V (TYP: 3.6V)
VDDIO_2P8	17	PO	2.8V power supply output	Output 50 mA at most, used only for level shifting. Add ESD protector when using this pin.
GND	1, 4, 10, 21			Ensure that all GND pins are connected to the ground.

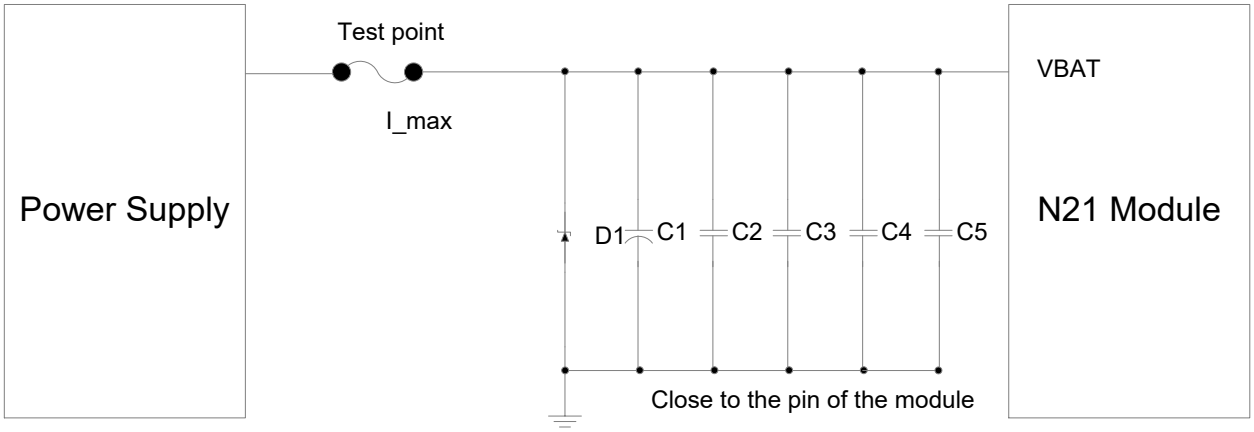
3.1.1 VBAT

The power supply design covers two parts: circuit design and PCB layout..

Circuit Design

N21 adopts a 3.3V-4.3V voltage input supplied by a battery and the typical voltage is 3.6V.Figure 3-1 Shows the reference design of N21 power supply.

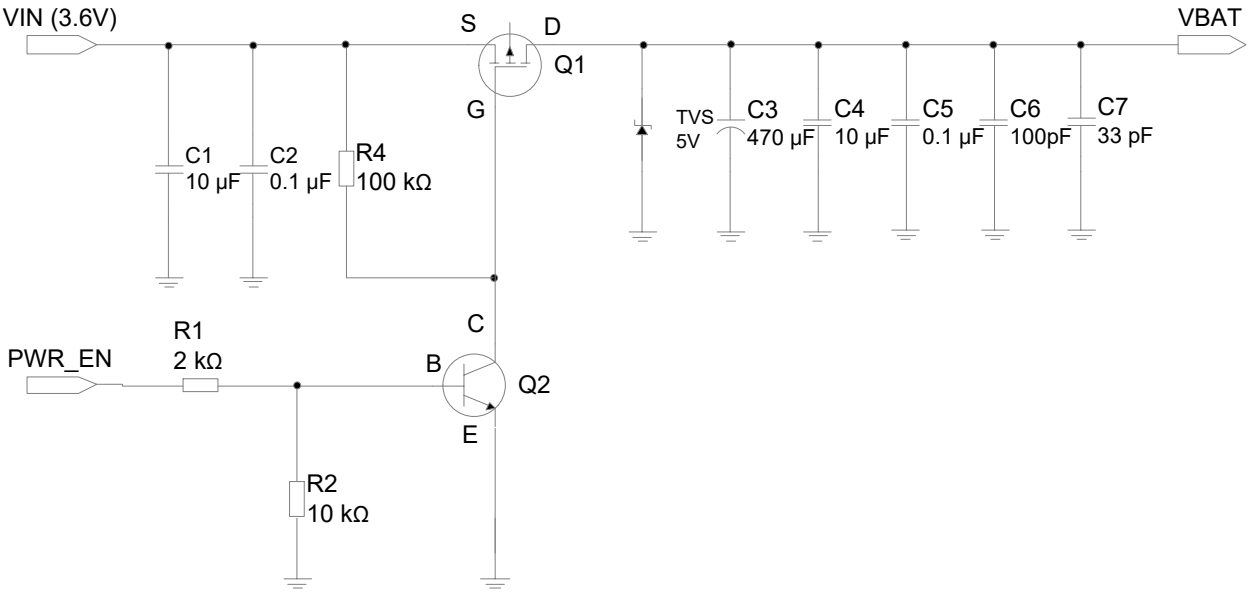
Figure 3-1 Recommended circuit design 1



- The maximum input voltage for the module is 4.3 V and the typical value is 3.6V.
- The protection voltage at D1 should not exceed the maximum input voltage the module can bear. Place TVS close to the input interface of the power supply to clamp the surge voltage before it enters back-end circuits. Therefore, the back-end components and the module are protected.
- A large bypass tantalum capacitor (220 μF or 100 μF) or aluminum capacitor (470 μF or 1000 μF) is expected at C1 to reduce voltage drops during bursts. Its withstand voltage should be larger than 1.5 times of the voltage across the power supply.
- Place a bypass capacitor of low-ESR close to the module to filter out high-frequency jamming from the power supply.

A controllable power supply is preferable if used in harsh conditions. Figure 3-2 shows the recommended circuit design.

Figure 3-2 Recommended circuit design 2



- Select an enhanced p-MOSFET at Q1, which has higher withstand voltage and drain current and low Rds.
- Select a common NPN tripolar transistor or a digital NPN tripolar transistor at Q2. Reserve enough tolerances of R1 and R2 in design, especially for the situation in which operating voltage of the tripolar might increase in low temperature.
- Place TVS2 close to the input interface of the power supply to clamp the surge voltage before it enters back-end circuits. Therefore, the back-end components and the module are protected.
- Place C1 close to the module. A large bypass tantalum capacitor (220 μF or 100 μF) or aluminum capacitor (470 μF or 1000 μF) is expected at C1 to reduce voltage drops during bursts. Its voltage rating should be larger than 1.5 times of the voltage across the power supply.
- Place a bypass capacitor of low-ESR close to the module to filter out high-frequency jamming from the power supply.

PCB Layout

Place an ESR capacitor at the output of the power supply to absorb surge current.Place a TVS diode at the input of VBAT to protect back-end components.The layout of components and PCB trace are critical to the hardware design of a device.Follow rules below in the power supply design:

- TVS diodes dissipate the transient pulse power during a surge and can handle a peak pulse current of dozens or more than 100 A. They have a fast response time. Place the TVS as close to the interface as possible to ensure that the surge voltage can be clamped before the pulse is coupled to the neighbor traces.
- Place bypass capacitors close to the power pin of the module to filter out the high-frequency signal from the power supply.
- Ensure that the width of PCB trances for VBAT circuits allows 1A current and ensure no obvious decrease of loop voltages. Trace width of VBAT should be at least 1mm and the ground level should be as complete as possible. The traces of power supply circuit should be as short and wide as possible.
- Noise-sensitive circuits such as audio and RF, should be placed far away from power supply circuits, especially when the DC-DC is adopted in the design. Connect GND pins and bottom pads to ground to optimize heat sink and separate noise.


Caution

Never use a diode to make the drop voltage between a higher input and module power. Otherwise, Neoway will not provide warranty for product issues caused by this. In this situation, the diode will obviously decrease the module performances, or result in unexpected restarts, due to the forward voltage of diode will vary greatly in different temperature and current. The module might not work properly with a diode power supply.

3.1.2 VDDIO_2P8

N21 provides one VDDIO_2P8 pin that outputs 2.8 V@50mA.

VDDIO_2P8 is enabled automatically when the module is awake or in running state.

It is recommended that VDDIO_2P8 is used for level shift only and an ESD protector should be added.

3.2 Control Interfaces

Signal	Pin	I/O	Function	Remarks
RESET_N	12	DI	Module reset input	Reset at low level
PWRKEY_N	5	DI	ON/OFF button	Triggered by low level to start or shut down the module.

3.2.1 PWRKEY_N

N21 allows startup by the following controls:

- Controlled by button
- Controlled by MCU
- Automatic start once powered up

Figure 3-3 Reference design of startup controlled by button

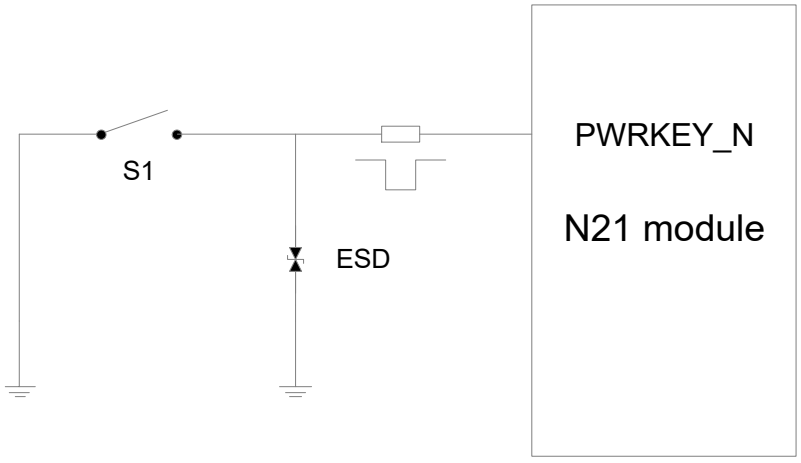


Figure 3-4 Reference design of startup controlled by MCU

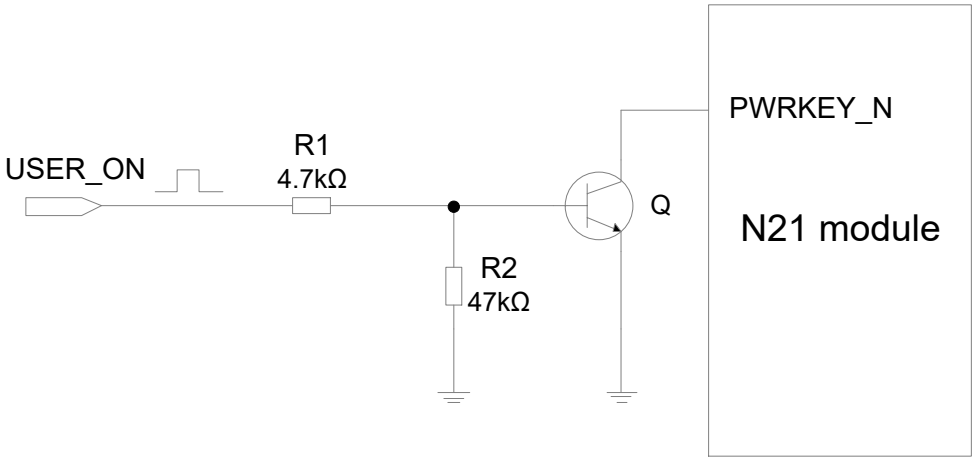
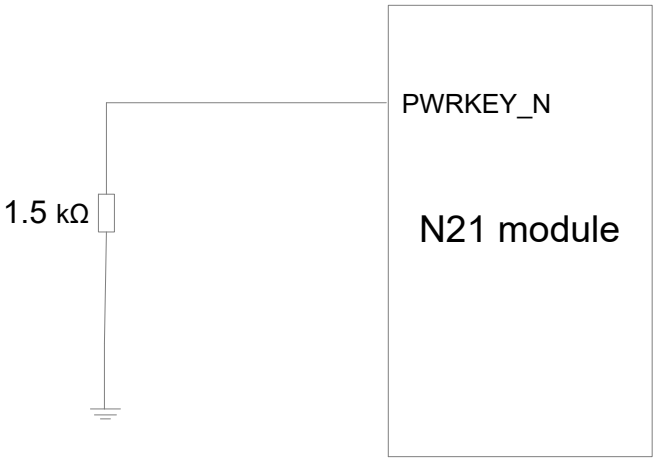


Figure 3-5 Reference design of automatic start once powered up



Startup Process

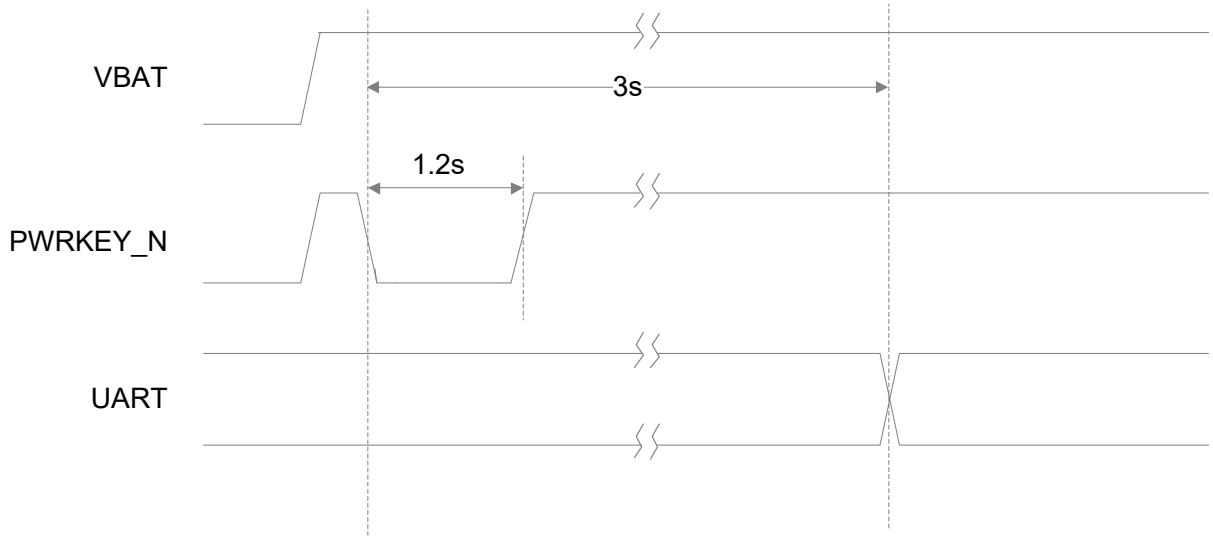
After powering up the VBAT pin, input low level for 1.2 second at PWRKEY_N to start the module.Pull PWRKEY_N to high level after the module is started.The STATUS indicator turns on, indicating that the module completes initialization.The baud rate of N21 is flexible since the module embeds automatic baud rate detection. Before sending data through UART port, issue AT so that the UART port can automatically detects the baud rate and outputs +PBREADY, indicating that the UART is ready.

In program design, use +PBREADY to check whether the module is reset due to any fault.

To use the function of automatic startup once powered up, refer to Figure 3-5. Note that this startup design does not support shutdown.

Prior to turning on the module, power on the host MCU and finish the UART initialization. Otherwise conflicts may occur during initialization, due to unstable conditions.

Figure 3-6 Startup timing



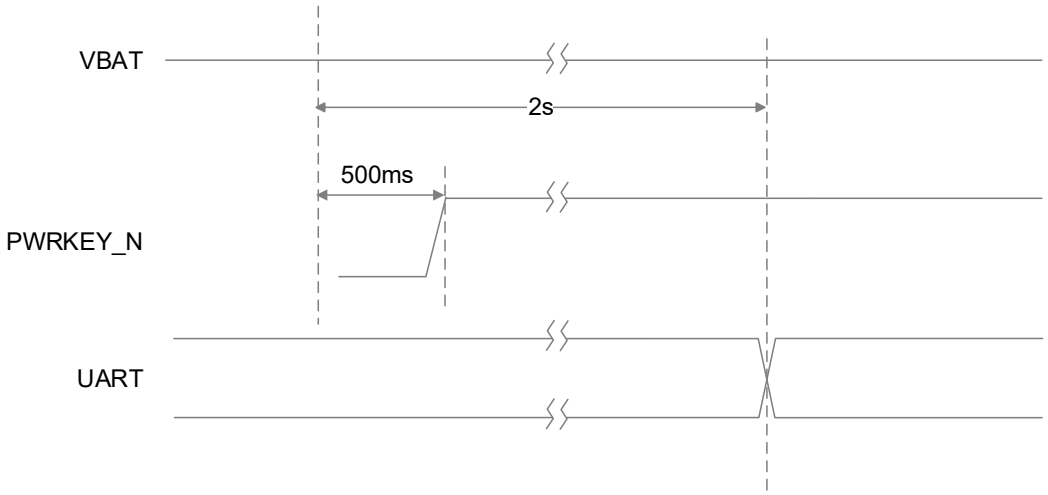
Shutdown Process

The module can be powered off in two ways: hardware power off and software power off.

PWRKEY_N is used to hardware shut down the module. When the module is working, inputting negative pulses for more than 500 ms to PWRKEY_N can trigger the shutdown process of the module. The module is shut down after around 2 seconds, and then turns off the power supply.

Figure 3-10 shows the hardware shutdown timing.

Figure 3-7 Shutdown timing



For how to power off through software, see *Neoway_N21_AT_Command_Manual*.

3.2.2 RESET_N

RESET_N is used to reset the module.RESET_N is used to hardware power off the module. When the module is working, inputting negative pulse for more than 200 ms to RESET_N can trigger the reset process of the module.

If you use a 2.8V/3.0V/3.3V IO system, it is recommended to add a triode to separate it. Refer to the following designs.To reset the module through high level, refer to Figure 3-4.

Figure 3-8 Reset controlled by button

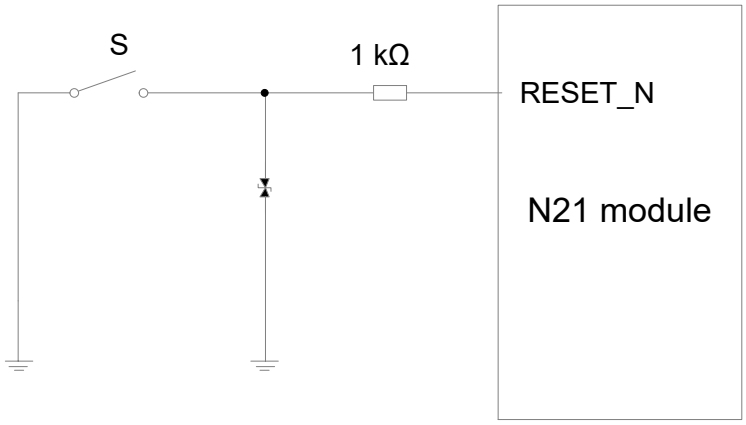
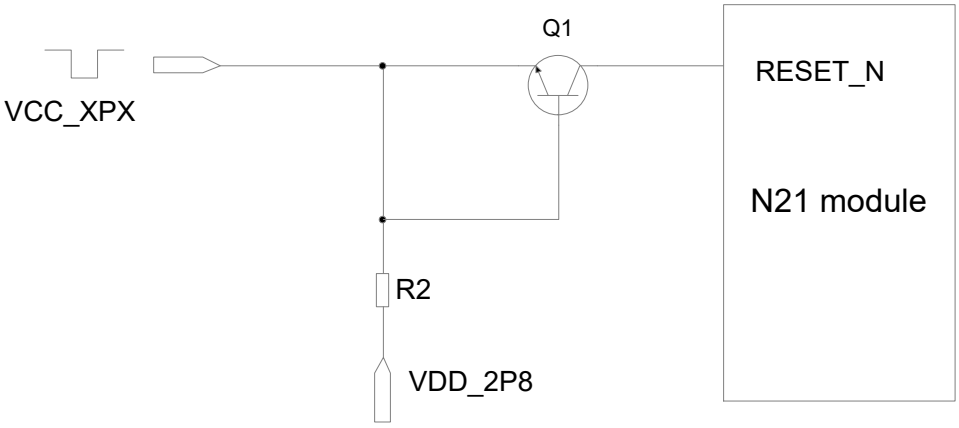


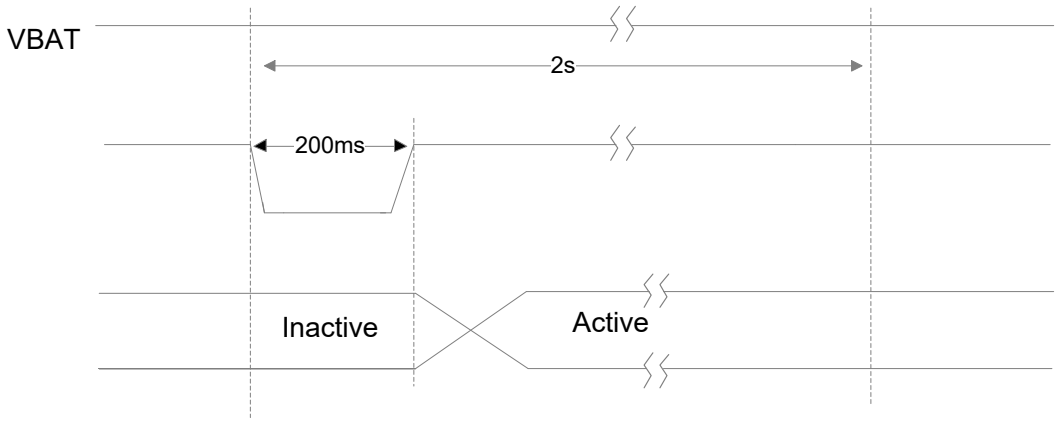
Figure 3-9 Reset circuit with triode separating



In a circuit shown in Figure 3-9, VDD_EXT=2.8V/3.3V/3.0V, R2=4.7KΩ.

The following figure shows the reset timing of N21.

Figure 3-10 Reset timing of N21



3.3 Peripheral Interfaces

N21 provides various peripheral interfaces.

Caution

In all reference designs of this section, the signals of pins on the module is named in perspective of module while peripheral pins are named from the view of the components. For example, UART_TXD indicates the pin that the module sends data while MCU_RXD indicates the pin that MCU receives data. These two pins should be connected.

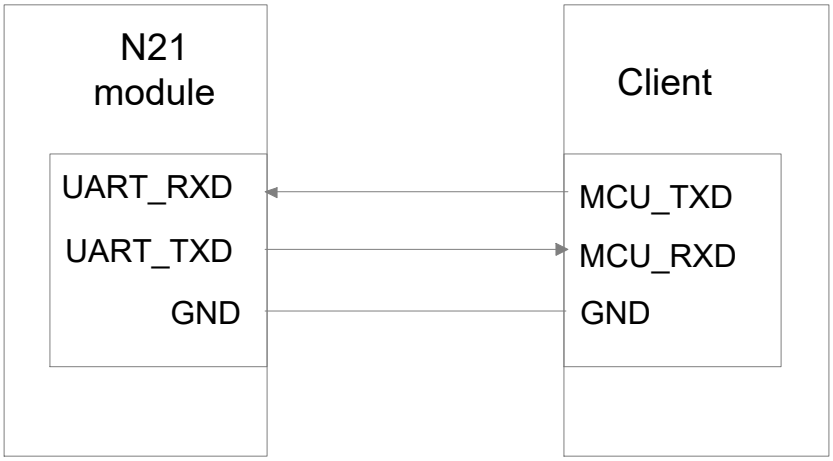
Please note the signal naming of pins on the components in peripheral selection and design.

3.3.1 UART

Signal	Pin	I/O	Function	Remarks
UART_TXD	14	DO	Data transmitting	
UART_RXD	13	DI	Data receiving	

N21 provides one UART interface that supports automatic baud rate detection. The level of the UART interface is 2.8V.

Figure 3-11 UART connection

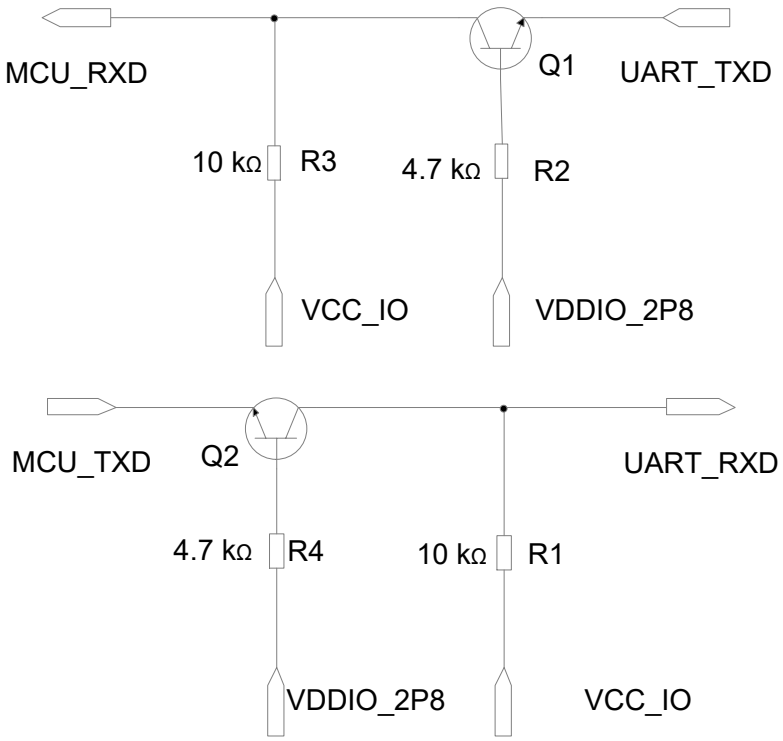


Circuit Design Cautions

- Note the match of signals.
- If the UART does not match the logic voltage of the MCU, add a level shifting circuit outside of the module. Three types of level shifting circuit is recommended based on the logic level quality.

If the low level at MCU_UART (V_{IL}) is lower than 200mV, adopt recommended level shifting circuit 1.

Figure 3-12 Recommended level shifting circuit 1

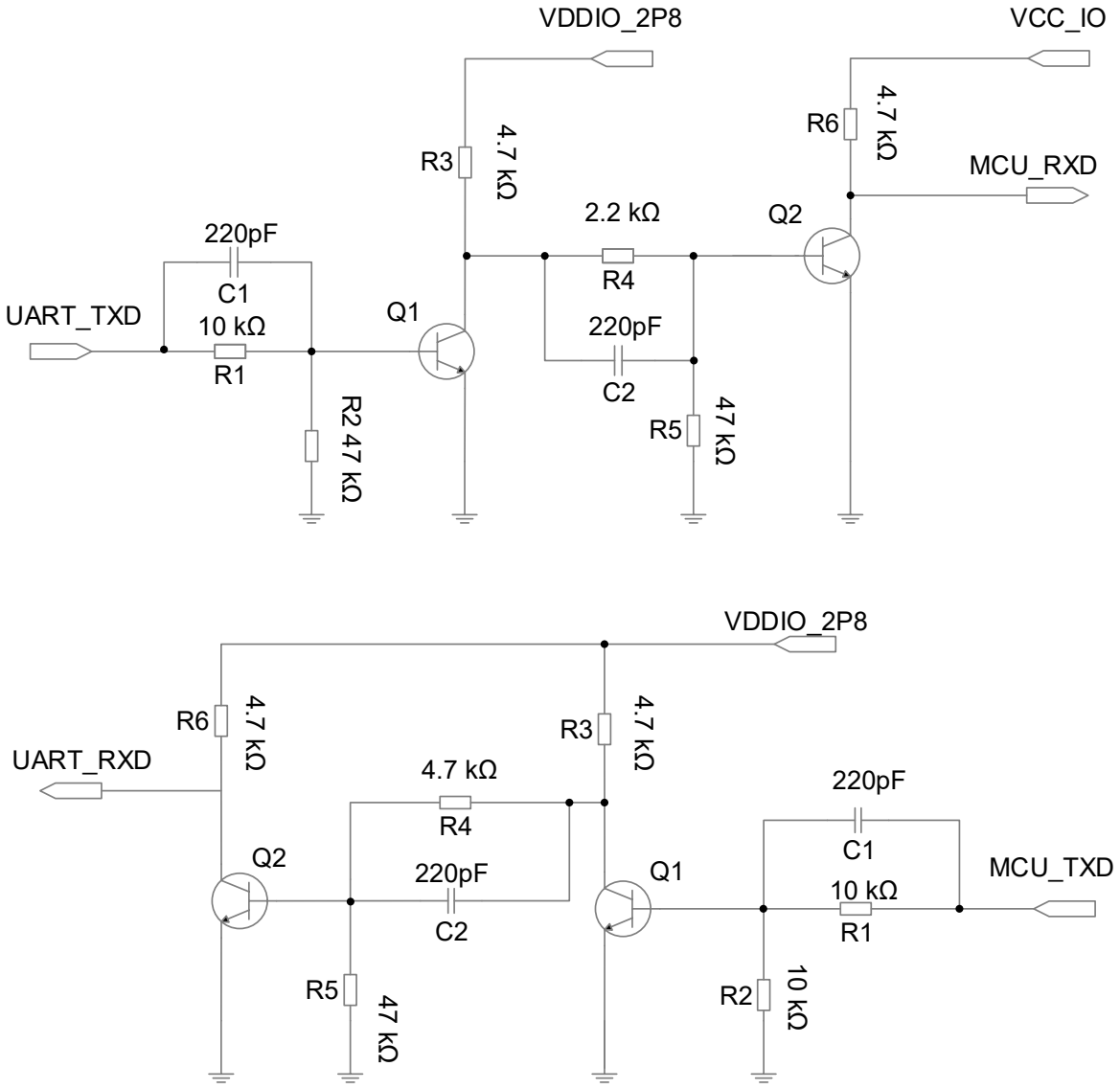


Components:

- R2, R4: 2KΩ-10KΩThe greater the UART baud rate is, the lower the R2 and R4 value is.
- R1, R3: 4.7KΩ-10KΩThe greater the UART baud rate is, the lower the R1 and R3 value is.
- Q1, Q2: MMBT3904 or MMBT2222. High-speed transistor is better.

If the low level at MCU_UART (V_{IL}) is lower than 200mV, adopt recommended level shifting circuit 2. Otherwise, low level at UART might be higher than required, resulting in failure to identify signals.

Figure 3-13 Recommended level shifting circuit 2

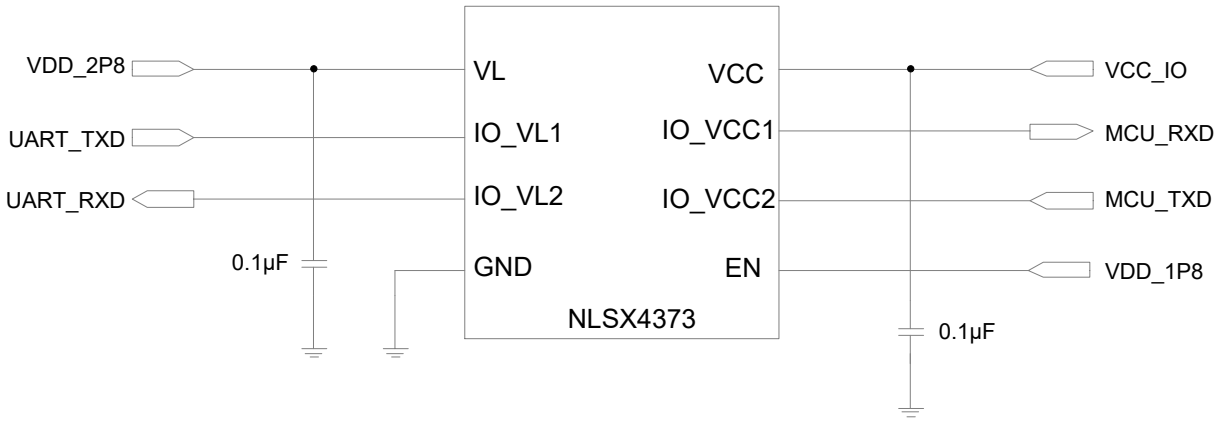


Q1, Q2: MMBT3904 or MMBT2222. High-speed transistor is better.

MCU_TXD and MCU_RXD are respectively the TX and RX of the MCU while UART_TXD and UART_RXD are respectively the TX and RX of the module.VCC_IO is the IO voltage of the MCU.

Level shift chip is recommended if the level of MCU is larger than 3.3V or the baudrate is higher than 1 MHz. 0 shows the reference design.

Figure 3-14 Recommended level shifting circuit 3



NLSX4373 is a dual-supply level shifter, the rate of which can be up to 20 Mb/s.

VL is the reference voltage of IO_VL1 and IO_VL2, ranging from 1.5V to 5.5V.

VCC is the reference voltage of IO_VCC1 and IO_VCC2, ranging from 1.5V to 5.5V.

EN is the enable pin, which works at a voltage of greater than VL-0.2V.

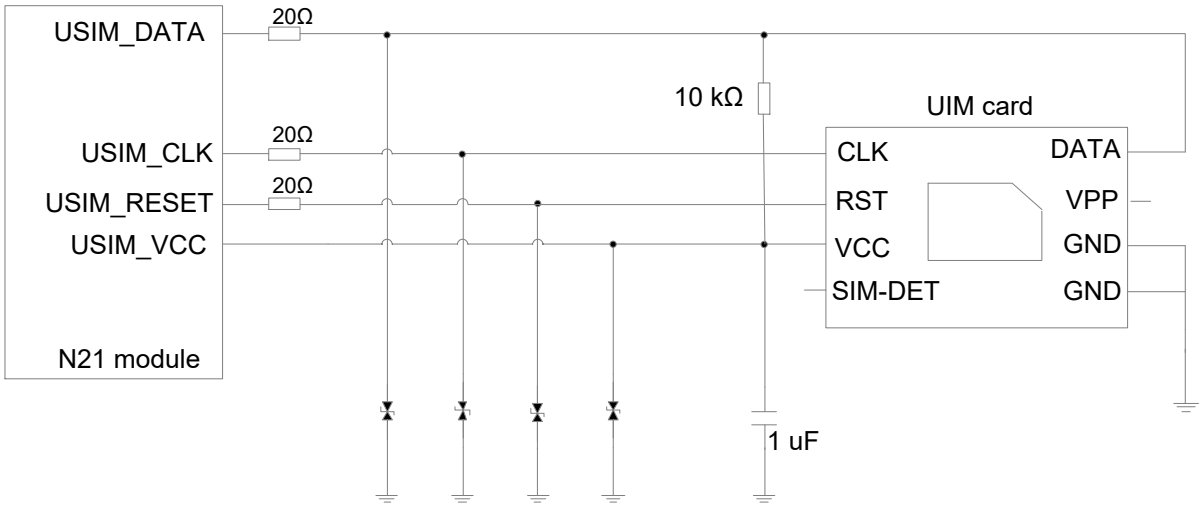
In the above circuit, the EN pin is connected to VDD_1P8 and the level shifter is always working.

3.3.2 USIM

Signal	Pin	I/O	Function	Remarks
USIM_VCC	9	PO	Power supply of USIM card	Compatible with 1.8 V/3 V USIM card
USIM_DATA	6	DIO	USIM card data IO	A 10 kΩ resistor is required between USIM1_VCC and USIM1_DATA.
USIM_CLK	7	DO	USIM clock	
USIM_RESET	8	DO	USIM reset	

N21 provides one USIM card interface that is compatible with 1.8V/3V USIM cards.Figure 3-15 shows the reference design of the USIM card interface.

Figure 3-15 Reference design of USIM card interface



Circuit Design Cautions

- USIM_VCC is the pin to supply power for SIM card and its maximum load is 30 mA. Do not use it for any other purpose.
- Reserve a position for pull-up resistor externally in design since the USIM_DATA pin is not pulled up internally.
- USIM_CLK is the clock signal pin, supporting a clock frequency of 3.25 GHz.
- Add ESD protectors, such as ESD diodes or TVS diodes (with a junction capacitance less than 33pF) on the USIM signal lines in applications with a high requirement of ESD protection.
- Connect a 20 Ω resistor respectively to USIM_DATA, USIM_RST, and USIM_CLK in series to enhance the ESD performance.

PCB Design Cautions

- USIM signals are like to be jammed by RF radiation, resulting in failure to detect the USIM card. Place USIM far away from RF circuits.
- Place USIM card closed to the module and USIM traces should be as short as possible.
- Place ESD protection resistors and components close to USIM card.
- Connect the ground of USIM to main ground to enhance jamming capability.

3.4 RF Interface

Signal	Pin	I/O	Function	Remarks
ANT	22	AI/O	Antenna	50Ω impedance

3.4.1 Antenna Design

ANT of N21 require a characteristic impedance of 50 Ω. Customers should control the impedance of the traces between the pins and antenna to ensure the RF performance. An impedance matching circuit, such as L network, split capacitor network, and pi network is mandatory in between. Pi network is recommended.

Figure 3-16 L network

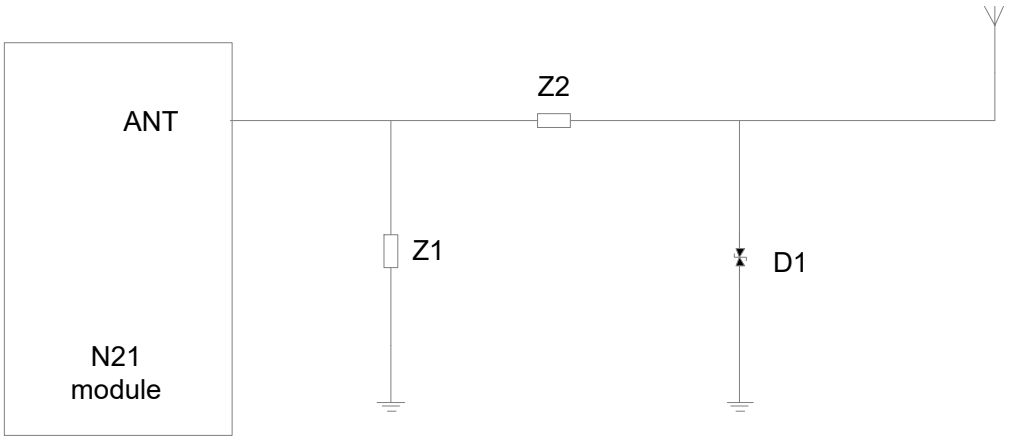


Figure 3-17 Split capacitor network

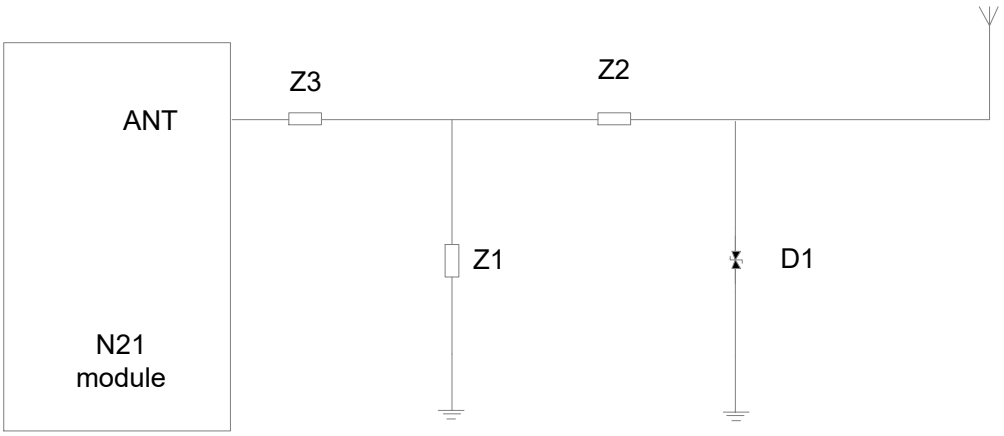
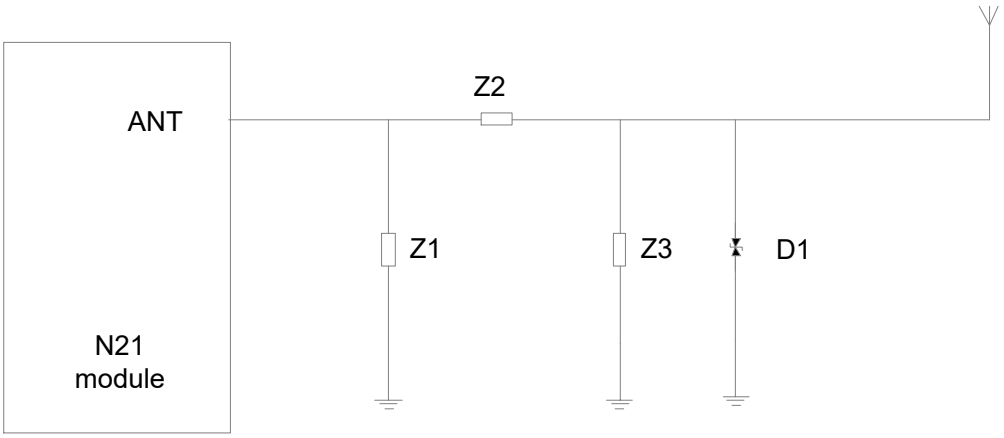


Figure 3-18 Pi network



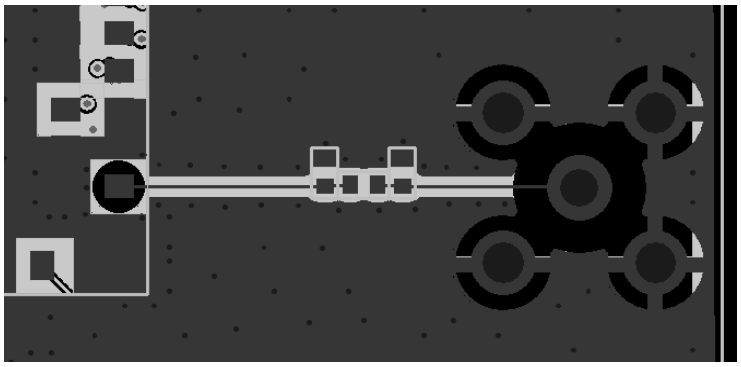
Circuit Design Cautions

- Element components in the above figures are capacitors, inductors, and 0Ω resistors. Place these RLC components as close to the antenna interface as possible.
- Add an ESD protector if the antenna might generate static electricity. The protector can be a TVS diode with a junction capacitance of lower than 0.5 pF. Ensure that the reverse breakdown voltage of the TVS is greater than 10V (above 15 V is recommended).

PCB Design Cautions

- Lay copper foil around RF connector. Dig as many ground holes as possible on the copper to ensure lowest grounding impedance.
- The traces between N21 and the antenna connector, should be as short as possible. Control the trace impedance to 50Ω.
- If customers adopt SMA connector, big RF solder pad might result in great parasitic capacitance, which will affect the antenna performance. Remove the copper on the first and second layers under the RF solder pad.

Figure 3-19 Recommended RF PCB design



- On the PCB, keep the RF signals and components far away from high-speed circuits, power supplies, transformers, great inductors, the clock circuit, etc.

3.4.2 Antenna Assembling

Antenna used for the module should meet the mobile device requirements: The VSWR ranges from 1.1 to 1.5 and the input input impedance is 50Ω. Antenna should be well matched to achieve best performance in different application scenarios.

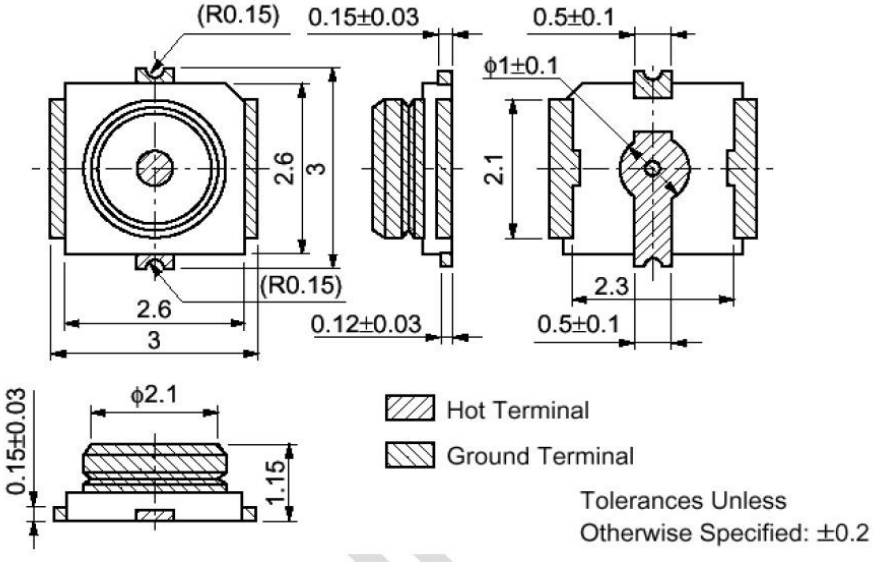
Antenna interfaces can be connected to rubber ducky antenna, magnet antenna, or embedded Planar Inverted F antenna (PIFA).Keep external RF wires far away from all disturbing sources, especially digital signals and DC/DC power if using RF wires.

The following methods are commonly used to assemble antenna:

- GSC RF connector

MM9329-2700RA1 from Murata is recommended. The following figure shows its encapsulation specifications.

Figure 3-20 Specifications of MM9329-2700RA1

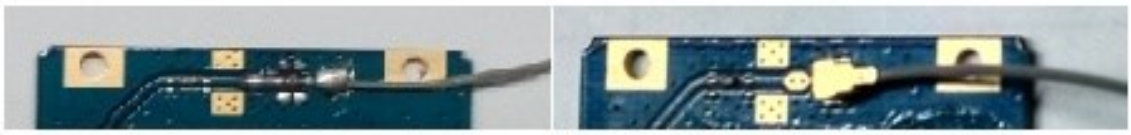


- Soldering

  RF wire can also be soldered to connect to the module. Ensure sufficient soldering in case of damage that lowers RF performance.

Figure 3-21shows the two types of connections.

Figure 3-21 RF connections



3.5 Other Interfaces

3.5.1 WAKEUP

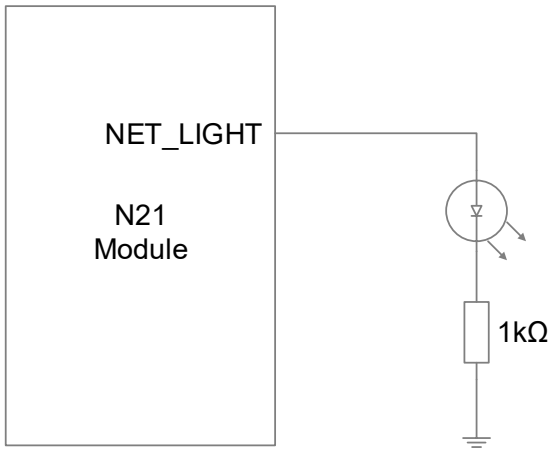
This pin is used to wake up N21 that is in PSM state.After N21 enters PSM state, input high level at WAKEUP pin for more than 1 second to wake up the module if any data is to send. However, the module will not register networks proactively after waken up. Therefore, users need to send a data transmitting request. For details, see *Neoway_N21_AT_Command_Manual*.

3.5.2 NET_LIGHT

NET_LIGHT outputs a high level of 2.8V and a maximum driving current of 4 mA.

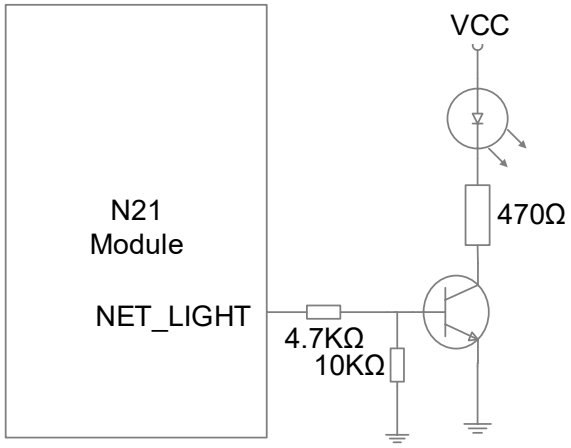
High level is allowed to drive a common LED indicator directly. See Figure 3-22.

Figure 3-22 Driving LED directly



For better luminance, drive the LED with a transistor instead. See 0.

Figure 3-23 Driving LED with a triode



For details, see *Neoway_21_AT_Command Manual*.

3.5.3 STATUS

STATUS is used to indicate that N21 is started up successfully.It can drive an LED indicator directly or through an triode.See Figure 3-22 and 0.

4 Electric Feature and Reliability

4.1 Nominal Values

Table 4-1 Operating conditions of N21

Pin	Parameter	Minimum Value	Typical Value	Maximum Value
VBAT	V_{in}	3.1V	3.6V	4.3V
	I_{in}	/	/	500mA

Caution

- If the voltage is too low, the module might fail to start. If the voltage is too high or there is a voltage burst during the startup, the module might be damaged permanently.
- If you use LDO or DC-DC to supply power for the module, ensure that it output at least 500mA current.

4.2 Current Features

Table 4-2 Current consumption of N21 (Typical)

Band \ Status	Power (dBm)	PSM (μA)	Idle (DRX/eDRX) (mA)	Active (mA)	
				TX	RX
Cat NB1: B3, B5, B8, B20, B28	23	<4.5	1.7/1	135	TBD
	0	<4.5	1.7/1	51	TBD
	-10	<4.5	1.7/1	36	TBD

4.3 Temperature Feature

Table 4-3 Temperature features of N21

Status	Minimum Value	Typical Value	Maximum Value
Operating	-30°C	25°C	75°C
Storage	-45°C		90°C

Caution

If the module works in an environment where the temperature exceeds the thresholds of the operating temperature range, some of its RF performance indicators might be worse but it can still work properly.

4.4 ESD Protection

Electronics need to pass ESD tests. The following table shows the ESD capability of key pins of this module. It is recommended to add ESD protection based on the application scenarios to ensure product quality when designing a product.

Humidity 45% Temperature 25°C

Table 4-4 N21 ESD protection

Testing Point	Contact Discharge	Air Discharge
VBAT	±8KV	±15KV
GND	±8KV	±15KV
ANT	±8KV	±15KV
Cover	±8KV	±15KV
Others	±2KV	±4KV

5 RF Features

5.1 Operating Band

Table 5-1 Operating band of N21

Operating Band	Uplink	Downlink
FDD-LTE B3	1710~1785MHz	1805~1880MHz
FDD-LTE B5	824~849MHz	869~894MHz
FDD-LTE B8	880~915MHz	925~960MHz
FDD-LTE B20	832~862MHz	791~821MHz
FDD-LTE B28	703~748MHz	758~803MHz

5.2 TX Power and RX Sensitivity

Table 5-2 RF TX power of N21

Band	Max Power	Min. Power
HD-FDD LTE B3	23dBm+2/-2dB	<-40 dBm
HD-FDD LTE B5	23dBm+2/-2dB	<-40 dBm
HD-FDD LTE B8	23dBm+2/-2dB	<-40 dBm
HD-FDD LTE B20	23dBm+2/-2dB	<-40 dBm
HD-FDD LTE B28	23dBm+2/-2dB	<-40 dBm

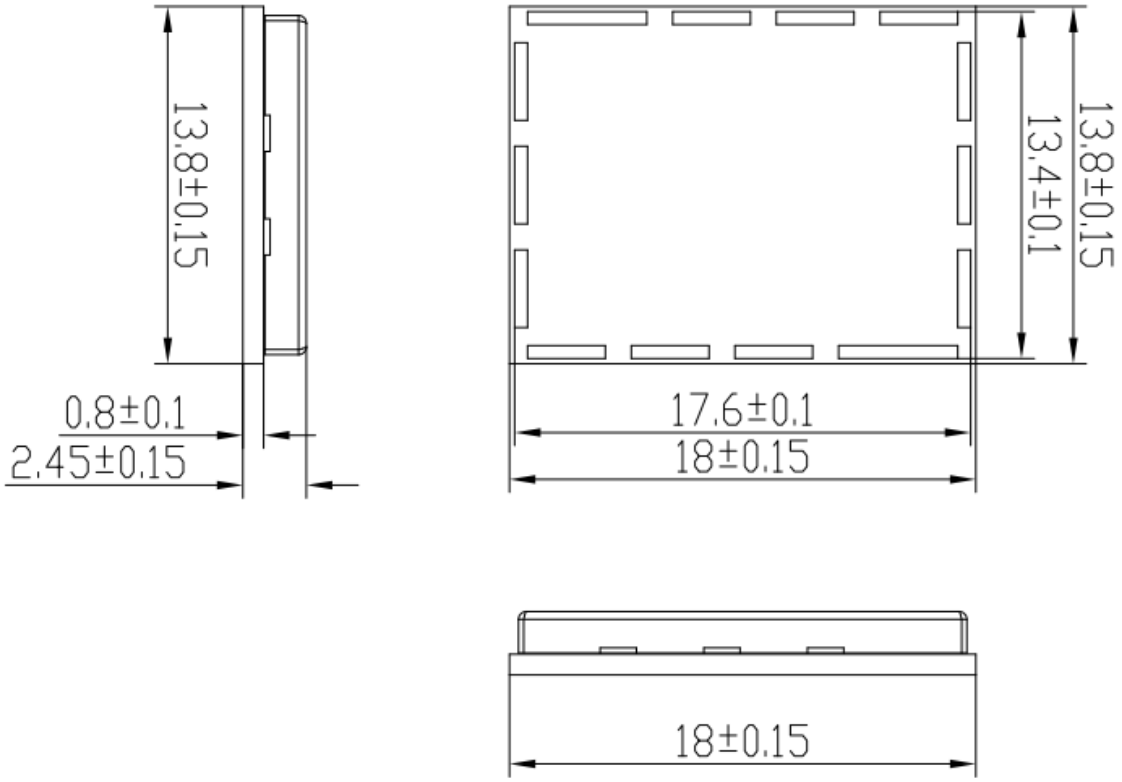
Table 5-3 RX sensitivity of N21 Cat NB1

Band	Sensitivity	Duplex Mode
LTE B3, B5, B8, B20, B28	≥-113dBm	HD-FDD

6 Mechanical Features

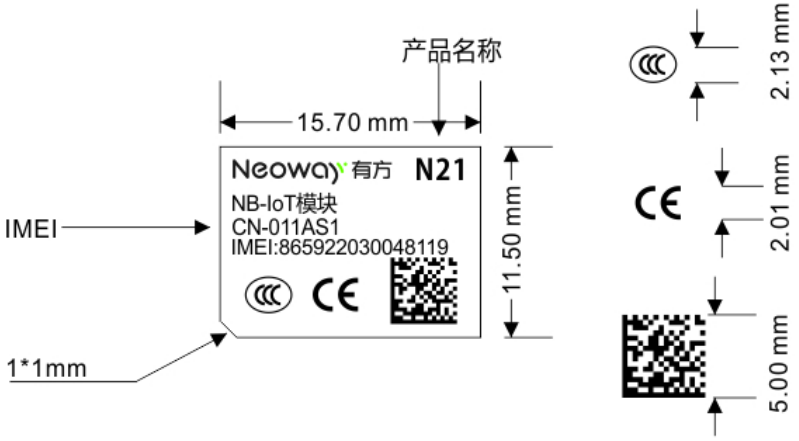
6.1 Dimensions

Figure 6-1 N21 dimensions (Unit: mm)



6.2 Label

The label is made of materials that are deformation-resistant, fade-resistant, and high-temperature-resistant and it can endure high temperature up to 260 °C.



Note

- The picture above is only for reference.
- The silk-screen printing must be clear. No blur is allowed.
- The material and surface finishing must comply with RoHS directives.

6.3 Package

N21 modules are packed in sealed bags on delivery to guarantee a long shelf life. Follow the same package of the modules again in case of opened for any reasons.

N21 is a level 3 moisture-sensitive electronic elements, in compliance with IPC/JEDEC J-STD-020 standard.

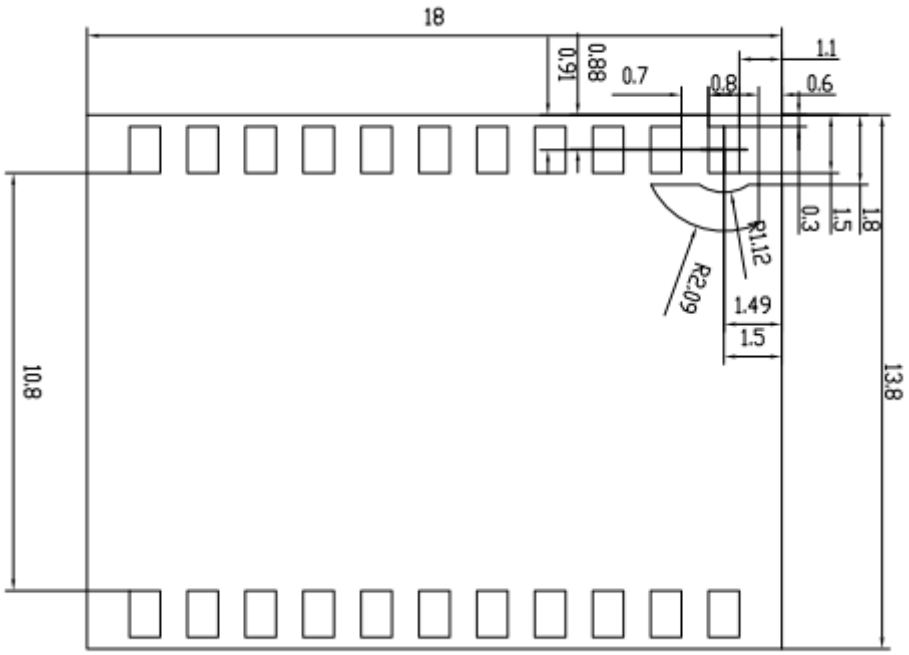
If the module is exposed to air for more than 48 hours at conditions not worse than 30°C/60% RH, bake it at a temperature higher than 90 degree for more than 12 hours before SMT.Or, if the indication card shows humidity greater than 20%, the baking procedure is also required.Do not bake modules with the package tray directly.

7 Mounting the Module onto the Application Board

N21 is introduced in 22-pin LGA package. This chapter describes N21 foot print, recommended PCB design and SMT information to guide users how to mount the module onto application PCB board.

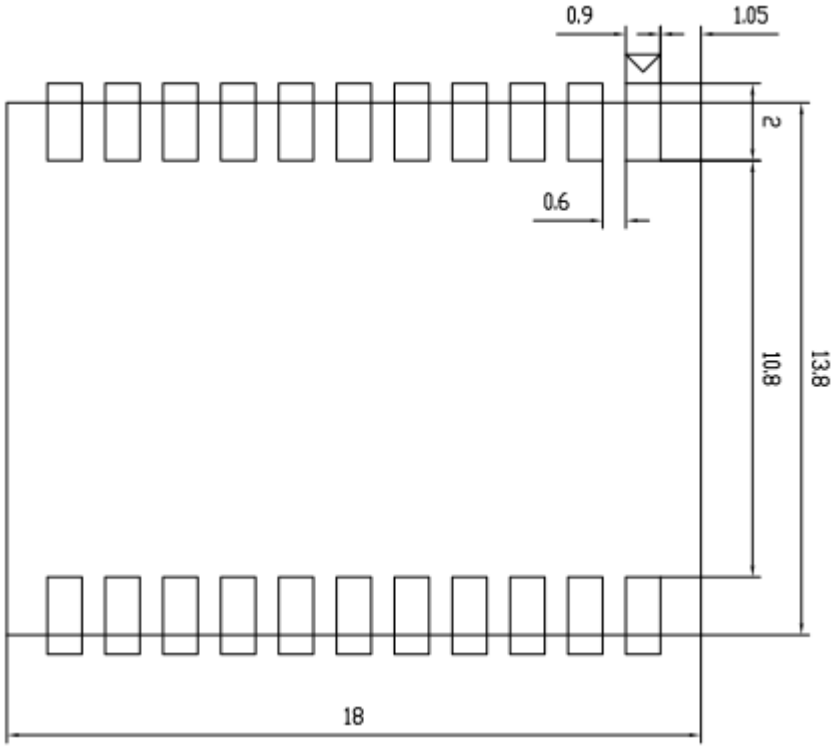
7.1 Bottom Dimensions

Figure 7-1 N21 bottom dimensions (Unit: mm)



7.2 Application Foot Print

Figure 7-2 Recommended PCB foot print (Unit: mm)



7.3 Stencil

The recommended stencil thickness is at least 0.12 mm to 0.15 mm.

7.4 Solder Paste

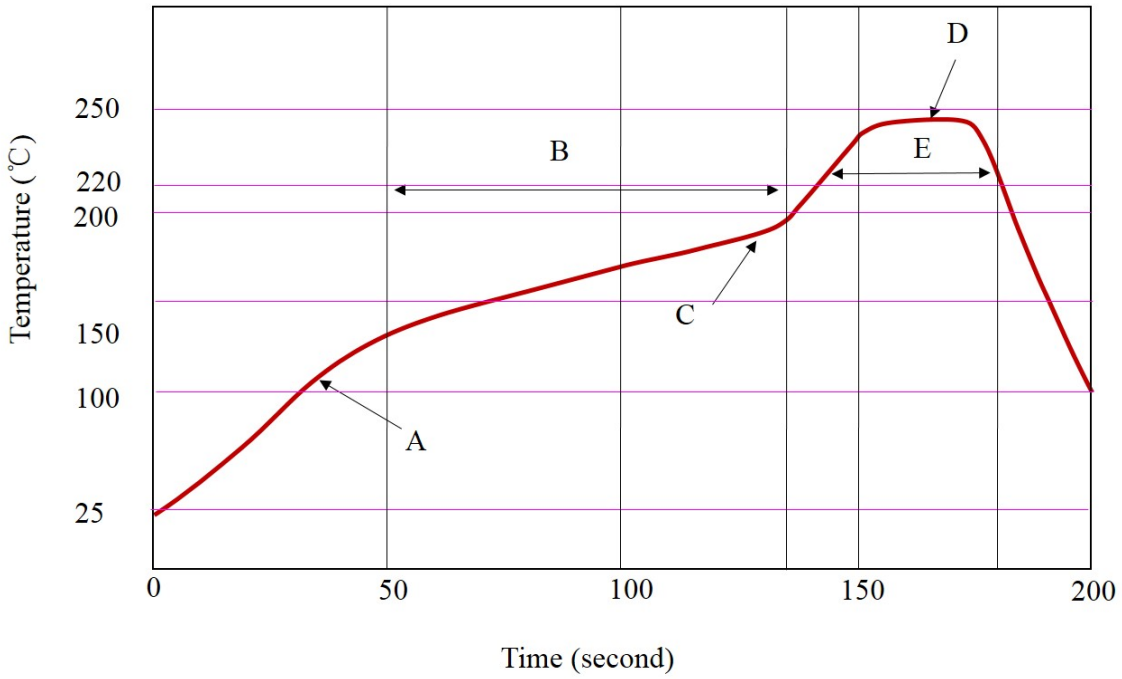
Do not use the kind of solder paste different from our module technique.

- The melting temperature of solder paste with lead is 35 °C lower than that of solder paste without lead. It is easy to cause voiding for LCC inside the module after second reflow soldering.
- When using only solder pastes with lead, please ensure that the reflow temperature is kept at 220 °C for more than 45 seconds and the peak temperature reaches 240 °C.

7.5 SMT Furnace Temperature Curve

Thin or long PCB might bend during SMT. So, use loading tools during the SMT and reflow soldering process to avoid poor solder joint caused by PCB bending.

Figure 7-3 SMT furnace temperature curve



Technical parameters:

- Ramp up rate: 1 to 4 °C/sec
  Ramp down rate: -3 to -1 °C/sec
- Soaking zone: 150-180 °C, Time: 60-100 s
- Reflow zone: >220 °C, Time: 40-90 s
- Peak temperature: 235-250 °C

Warning

Neoway will not provide warranty for heat-responsive element abnormalities caused by improper temperature control.

For information about cautions in N21 storage and mounting, refer to *Neoway Module Reflow Manufacturing Recommendations*.

When manually desoldering the module, use heat guns with great opening, adjust the temperature to 250 degrees (depending on the type of the solder paste), and heat the module till the solder paste is melt. Then remove the module using tweezers. Do not shake the module in high temperatures while removing it. Otherwise, the components inside the module might get misplaced.

8 Safety Recommendations

Ensure that this product is used in compliant with the requirements of the country and the environment. Please read the following safety recommendations to avoid body hurts or damages of product or work place:

- Do not use this product at any places with a risk of fire or explosion such as gasoline stations, oil refineries, etc
- Do not use this product in environments such as hospital or airplane where it might interfere with other electronic equipment.

Please follow the requirements below in application design:

- Do not disassemble the module without permission from Neoway. Otherwise, we are entitled to refuse to provide further warranty.
- Please design your application correctly by referring to the HW design guide document and our review feedback on your PCB design. Please connect the product to a stable power supply and lay out traces following fire safety standards.
- Please avoid touch the pins of the module directly in case of damages caused by ESD.
- Do not remove the USIM card in idle mode if the module does not support hot plugging.

A Conformity and Compliance

A.1 Approvals

- CCC
- SRRC
- CTA
- RoHS
- CE*
- GCF*
- Vodafone*
- FCC*
- China Mobile/China Unicom/China Telecom
- Ali cloud*

A.2 Chinese Notice

A.2.1 CCC Class A Digital Device Notice

This product has been tested and found to comply with the limits for class A digital devices.These limits are designed to provide reasonable protection against harmful interference in a residential installation.

A.2.2 Environmental Protection Notice

This product is in compliant with China RoHS directives and does not contain any hazardous substances as per the above referenced standard. Follow the regulations of the countries when storing, applying, and discarding it.

A.3 American Notice

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and

(2) this device must accept any interference received, including interference that may cause undesired operation.

A.3.1 Modify

Changes or modifications made to this equipment, not expressly approved by us or parties authorized by us could void the user's authority to operate the equipment.

A.3.2 FCC Class A Digital Device Notice

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protectionagainst harmful interference in a commercial environment.This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

A.3.3 FCC Class B Digital Device Notice

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protectionagainst harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

B Abbreviation

Abbreviation	English Full Name
ADC	Analog-Digital Converter
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DCE	Data Communication Equipment
DTE	Data Terminal Equipment
PTW	Paging Time Window
PSM	Power Save Mode
DRX	Discontinuous Reception
eDRX	Extended Discontinuous Reception
EMC	Electromagnetic Compatibility
EMI	Electro Magnetic Interference
ESD	Electronic Static Discharge
ETSI	European Telecommunication Standard
FDMA	Frequency Division Multiple Access
IC	Integrated Circuit
IMEI	International Mobile Equipment Identity
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MS	Mobile Station
PCB	Printed Circuit Board
RAM	Random Access Memory
RF	Radio Frequency
ROM	Read-only Memory
TVS	Transient Voltage Suppressor

RTC	Real Time Clock
USIM	Subscriber Identification Module
SRAM	Static Random Access Memory
TDMA	Time Division Multiple Access
UART	Universal asynchronous receiver-transmitter
VSWR	Voltage Standing Wave Ratio